## REMARKS

The Examiner is thanked for the thorough examination of the present application and the withdrawal of all previous rejections. The Office Action, however, has continued to reject all claims. Specifically, the Office Action has now rejected claims 1, 3-6, and 8-19 under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. publication 2004/0260908 to Malik. Applicants respectfully submit that the rejections be reconsidered and withdrawn for at least the reasons set forth herein.

**Independent Claim 1 (and dependent claims 3-5)**

Turning now to the substantive rejections, claim 1 (as amended) recites:

> 1. A method comprising:
> determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the first I/O device and a memory device;
> buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, ***a size of the first portion being responsive to the at least one characteristic of the first I/O device***;
> ***determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and***
> ***buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device***.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that Malik fails to disclose the features emphasized above.

To assist the Examiner's understanding of claim 1, with reference to the specification and drawings, claim 1 defines: a method comprising determining at least

one characteristic (see e.g., at least Figs. 2A and 2B, p. 5, line 16 ~ bottom of p. 6 of the specification) of a first input/output (I/O) device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) that is coupled to a memory device (see e.g., Fig. 1A, element 106, p. 3, lines 12-26) (see e.g., Fig. 1A, element 102, p. 3, lines 12-26), the memory device interface being configured to enable data transfers between the first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) and a memory device (see e.g., Fig. 1A, element 104, p. 3, lines 12-26). The method further comprises buffering data corresponding to the first I/O device (see e.g., Fig. 1A, element 102, p. 3, lines 12-26) in a first portion of a buffer of the memory device interface (see e.g., Fig. 1A, element 104, p. 3, lines 12-26), a size of the first portion being responsive to the at least one characteristic of the first I/O device (see e.g., p. 5, line 23~ p. 6, line5), and determining at least one characteristic of a second I/O device (see e.g., p. 5, line 19, reciting multiple I/O devices 102) that is coupled to the memory device interface. In addition, the method comprises buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.

First, Applicants note that the Office Action has not clearly applied the teachings of Malik. For example, claim 1 defines two instances of "determining" and "buffering" operations, in relation to a characteristic of a "first I/O device" and a "second I/O device." For both sets of the operations, however, the Office Action has applied the same, general teachings of Malik. That is, the Office Action stated that the first "determining" and "buffering" operations were disclosed by paragraphs 13-16, 19, and figures 1, 2, and 5. Likewise, the Office Action stated that the second

"determining" and "buffering" operations were disclosed by the exact same portions of Malik. Unfortunately, the Office Action did not state what (in Malik) constituted the first I/O device or what constitute the second I/O device. Similarly, the Office Action did not state what allegedly constitutes the "characteristic" of the I/O devices. As the cited teachings (paragraphs 13-16 and 19) span over two entire columns of text, it has made it difficult to accurately (and with certainty) assess the Office Action's application of Malik.

In total, the cited portion of Malik states:

> [0013] FIG. 1 illustrates in block diagram form a data processing system 10 generally having a plurality of data processors that function as a bus master of the data processing system 10. A first master 12, a second master 14 and a third master 16 are each connected to interconnect circuitry 18 that contains switch circuitry 19. Master 12, master 14 and master 16 function as bus masters and selectively have sole control of the bus formed by the memory controller interconnect between switch circuitry 19 and memory controller 20. In one form, the switch circuitry 19 is implemented as a crossbar switch. The crossbar switch conventionally contains an address decoder and a mechanism for bus arbitration to grant any one of masters 12, 14 and 16 access to a memory controller 20. Data processing system 10 further contains a first memory 22, a second memory 24 and a third memory 26, each of which is connected to the memory controller 20. Data processing system 10 also contains one or more additional slave devices 28. Examples of the other slave device(s) 28 include a timer, an LCD controller, etc. Memory controller 20 contains a prefetch buffer 30 and prefetch control circuitry 32. The first master 12 has various signaling or interconnect provided between switch circuitry 19. A master identifier or master identification (ID) signal is connected from the first master 12 to switch circuitry 19. A data size 1 signal is connected from the first bus master 12 to switch circuitry 19. One or more control signals in the form of other control 1 signal(s) are connected from the first bus master 12 to switch circuitry 19. A burst length 1 signal is connected from the first master 12 to switch circuitry 19. A bi-directional address/data 1 bus is connected between the first master 12 and switch circuitry 19. This interconnect collectively form a master 1 interconnect. Similar master interconnect signaling is connected between each of the masters 14 and 16 and the switch circuitry 19 and are not shown in detail simply for purposes of convenience of illustration. A memory controller interconnect is connected between the switch circuitry 19 and the memory controller 20. A Master Identification (ID) signal bus is connected from switch circuitry 19 to memory controller 20. A Data Size signal bus for providing a data size indicator is connected from switch circuitry 19 to memory controller 20. A Burst Length signal bus for providing a burst length indicator is connected from switch

circuitry 19 to memory controller 20. A signal bus labeled `Other Controls` is connected from switch circuitry 19 to memory controller 20 for providing a variety of additional control information from the selected bus master to memory controller 20. A bidirectional Address/Data bus is connected between switch circuitry 19 and memory controller 20. Between each of memory 22, 24 and 26 and memory controller 20 is a memory interconnect. For example, a first memory interconnect is connected between memory controller 20 and first memory 22. A bus width signal is connected from the first memory 22 to the memory controller 20. A multi-bit bi-directional Address/Data/Control bus is connected between first memory 22 and memory controller 20. In the illustrated form, the second memory interconnect and the third memory interconnect are the same as the first memory interconnect but are not shown in detail for convenience of illustration.

[0014] In operation, any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. In response, the interconnect circuitry 18 grants ownership of the memory controller interconnect to the requesting master. The read request from the master is seen by the memory controller 20. The read request has one or more attributes such as the Data Size and Burst Length. The memory controller is aware of the master ID, the data size being requested and a requested burst length as well as a memory address. The Burst Length signal communicates to the memory controller 20 whether the requested operation is a burst operation. Based on the information in the memory controller interconnect, if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. Status bits in the prefetch buffer 30, to be described below, are accordingly updated.

[0015] If the address does not hit in the prefetch buffer 30 and misses, based on whether the requesting master is enabled for prefetching, dynamic configuration of the prefetch buffer line size occurs based on data size and burst length. An adaptive buffer line replacement algorithm, to be described below, selects which buffer line is replaced and new data written to. The prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

[0016] Illustrated in FIG. 2 is a diagram of a portion of a configuration of the prefetch buffer 30 based upon different burst length support. In the illustrated form, a plurality of burst blocks or burst lines, such as burst lines 36, 38, 40, 42, 44 and 46, is provided. Burst lines 36 and 38 support eight word (i.e. thirty-two bit words) burst operation. Within each burst line, such as burst line 36 is a status field and a predetermined number of data words in a data field 50. Prefetch buffer 30 is configured for eight word burst operation in each of burst lines 36 and 38, whereas prefetch buffer 30 is configured for four word burst operation in each of burst lines 40, 42, 44 and 46. Because there are two different sizes of burst lines, it is clear that the master is supporting at least two lengths of memory bursting, or conversely, that different bus masters support different burst lengths. It should be understood that the data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26 than the data from burst line 36. The same is true with respect to the source of data in all of the other illustrated burst lines. The particular

configuration of prefetch buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and the Burst Length signal. The Data Size signal determines the size of a single unit of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. In FIG. 2, the Data Size signal selects a data size being a word in length. Other data sizes such as multiple words or a byte could be indicated by the Data Size signal. The Burst Length signal allows the use of different types of bus masters to be implemented in data processing system 10. For example, if the first master 12 only supports bursts of eight words in length and the second bus master 14 supports bursts of four words in length, the prefetch buffer configuration of FIG. 2 will support both of these bus masters. In contrast, previous systems would require separate storage elements with predetermined fixed configurations to separately support the two differing bus masters. It should be noted that in the illustrated portion of prefetch buffer 30 of FIG. 2, the buffer storage area is dynamically configurable, based on the requested accesses to be serviced. Thus, although the illustrated configuration contains two burst line buffers holding eight words each and four burst line buffers holding four words each, depending on the history and type of burst requests, the buffers may be dynamically configured into any combination of lengths as access requests are received. Dynamic configuration of the buffers may be based at least in part on the Data Size and Burst Length signals.

...

[0019] Illustrated in FIG. 5 is a further detail of one implementation 70 of the prefetch control circuitry 32 of FIG. 1. Dynamic Buffer Configuration logic 72 has a first input for receiving the Data Size attribute signal, a second input for receiving the Burst Length attribute signal, a third input for receiving the Bus Width signal from an addressed memory, such as memory 22, 24 or 26. A first output of the Dynamic Buffer Configuration logic 72 is connected to an input of Adaptive Buffer Store Replacement logic 74. An output of the Adaptive Buffer Store Replacement logic 74 provides a buffer portion replacement indicator and is connected to a first input of Request Type logic 76. A second output of the Dynamic Buffer Configuration logic 72 is connected to a second input of the Request Type logic 76. An output of the Request Type logic 76 is connected to one of the three Memory Interconnects of FIG. 2.

Although the Office Action has not explained the rejection, it appears that the memory controller 20 of Malik is being applied as the claimed "memory device interface," and that the memories 22, 24, and 26 are being applied as the claimed first and second "memory I/O devices." It also appears that the "prefetch buffer 30" of Malik is being applied as the claimed "buffer" of the memory device. Assuming that this understanding is correct, claim 1 still requires "*a size of the first portion being*

*responsive to the at least one characteristic of the first I/O device*;" "*determining at least one characteristic of a second I/O device that is coupled to the memory device interface;" and "buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device*." Simply stated, no such features are disclosed in Malik.

With regard to these features of claim 1, it appears that the Office Action may be relying on the teaching of FIG. 5, and the related description of paragraph [0019], which has been set forth above. In this portion, Malik discloses a dynamic buffer configuration. Significantly, however, there is no disclosure in Malik of a size of the first portion of the buffer being responsive to a characteristic of one of the memories 22, 24, or 26 (the memories presumably being equated to the claimed I/O devices), much less a size of a second portion of the buffer being responsive to a characteristic of another of the memories 22, 24, or 26. Consequently, Malik does not anticipate the combination defined by claim 1, and for at least these reasons, the rejections of claim 1 should be withdrawn.

Further still, each of independent claims 6, 10, 15, and 19 recite:

> 6. A method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising:
> buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface;
> buffering data received via a second data transfer link in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion; and
> ***wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that***

***provides data to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link.***

10. A memory device interface that is configured to enable data transfers between an input/output (I/O) device, the memory device interface comprising:

a buffer;

a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device; and

***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer.***

15. A memory device interface comprising:

a buffer;

a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link; and

***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link, a size of the first portion of the buffer being different than a size of the second portion of the buffer.***

19. A system comprising:

means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device;

means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;

***means for determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and***

***means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion***

***being responsive to the at least one characteristic of the second I/O device.***

(*Emphasis added.*) Each of these claims patently defines over Malik for at least the reason that Malik fails to disclose the features emphasized in those claims above. In this regard, the features emphasized above loosely correspond to the defining features of claim 1, and the Office Action has rejected these claims on the same basis as claim 1 (citing the same paragraphs 0013-0016 and 0019. Furthermore, as the Office Action has not specifically applied the teachings of Boyle to the language of these claims, Applicant submits that the outstanding rejections of these claims cannot be sustained.

Further still, with respect to claim 19, Applicant notes that the elements of claim 19 are set forth in means-plus-function format. Even though the elements may loosely correspond to the claim elements of claim 1, they cannot properly be construed coextensively. Instead, pursuant to 35 U.S.C. § 112(6), a claim element recited in means-plus-function format "shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. § 112, ¶ 6. The Federal Circuit has clearly endorsed this statutory mandate by holding that claims interpreted under 35 U.S.C. § 112, paragraph 6, are limited to the corresponding structure disclosed in the specification and it equivalents. Kahn v. General Motors Corp. 135 F.3d 1472, 45 U.S.P.Q.2d 1608 (Fed. Cir. 1998).

There should be no question but that the elements recited in claim 29 are to be construed pursuant to 35 U.S.C. § 112, paragraph 6. In Greenberg v. Ethicon Endo-Surgical Inc., 91 F.3d 1580, 39 U.S.P.Q. 2d 1783 (Fed. Cir. 1996), the Federal Circuit stated that the use of "means for" language generally invokes 112(6). Indeed, only if

means plus function claim elements recite sufficient structure to carry out the function are that taken out of the gambit of 35 U.S.C. § 112, paragraph 6. Cole v. Kimberly-Clark Corp., 102 F.3d 524, 41 U.S.P.Q.2d 1001 (Fed. Cir. 1996).

Indeed, the Federal Circuit reiterated in Sage Products, Inc. v. Devon Industries, Inc., 126 F.3d 1420, 44 U.S.P.Q.2d 1103 (Fed. Cir. 1998) that "the use of the word 'means,' which is part of the classic template for functional claim elements, gives rise to 'a presumption that the inventor used the term advisedly to invoke the statutory mandates for means-plus-function clauses." Ultimately, the Court in Sage construed the relevant claim elements under 35 U.S.C. § 112(6), because 'means' were recited, and the claim elements did not "explicitly recite[s] the structure, material, or acts needed to perform the [recited] functions. Sage at p. 1428. The Federal Circuit further acknowledged this presumption in Al-Site Corp. v. VSI International, Inc., 174 F.3d 1308, 50 U.S.P.Q.2d 1161 (Fed. Cir. 1999).

Thus, claim elements expressed in "means" plus function format are construed as determined in accordance with 35 U.S.C. § 112, paragraph 6, as set forth above, and as further described in *In re Donaldson* 16 F.3d 1189, 29 U.S.P.Q.2d 1845 (Fed. Cir. 1994)(*en banc*). Therefore, the various means elements of claim 19 must be construed in accordance with the corresponding structure set forth in the present specification. In this regard, Applicants note that, in *In re Donaldson*, The Board of Patent Appeals and Interferences advanced the legal proposition that "limitations appearing in the specification are *not* to be read into the claims of an application." *In re Donaldson* at 1848. This argument, however, was rejected by the Federal Circuit, which held, as a matter of law, that "one construing means-plus-function language in a claim must look to the

specification and interpret that language in light of the corresponding structure ... described therein, and equivalents thereof. *In re Donaldson* at 1848. Furthermore, the holding in *In re Donaldson* does not conflict with the principle that claims are to be given their broadest reasonable interpretation during prosecution. *In re Donaldson* at 1850.

Accordingly, the fact that the Office Action appears to have construed the claim element of claim 19 to be co-extensive with the claim elements of claim 1 constitutes legal error. Simply stated, the rejection of claim 19 is erroneous, and must be withdrawn.

Claims 6-7 depend from independent claim 5, claims 11-14 depend from independent claim 10, and 16-18 depend from independent claim 15. As dependent claims include all of the features of the base claims from which they depend, the rejection of dependent claims 6-7, 11-14, and 16-18 should be withdrawn for at least the same reasons as those advanced above in connection with the independent claims.

**CONCLUSION**

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

/Daniel R. McClure/

Daniel R. McClure
Registration No. 38,962

(770) 933-9500

Please continue to send all future correspondence to:

Hewlett-Packard Development Company, L.P.
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400